

FIGURE 1

The diagram illustrates a 'RESETTABLE MEMORY' (220) composed of two memory units and a multiplexer:

- MEMORY UNIT WITH RESET (205):**
 - Inputs: RESET (219), DATA IN (214), WE, ADDR, RE.
 - Output: DATA OUT (210).
- MEMORY UNIT WITHOUT RESET (201):**
 - Inputs: WE (204), ADDR (202), DATA IN (203, n-bit), RE (230).
 - Output: DATA OUT (206).
- Multiplexer (207):**
 - Inputs: DATA OUT (210) from unit 205, and DATA OUT (206) from unit 201.
 - Control: 'reset value' (208) selects between inputs 0 and 1.
 - Output: DATA OUT (209).

The entire assembly is labeled **RESETTABLE MEMORY 220**.

FIGURE 2A

100133-03000

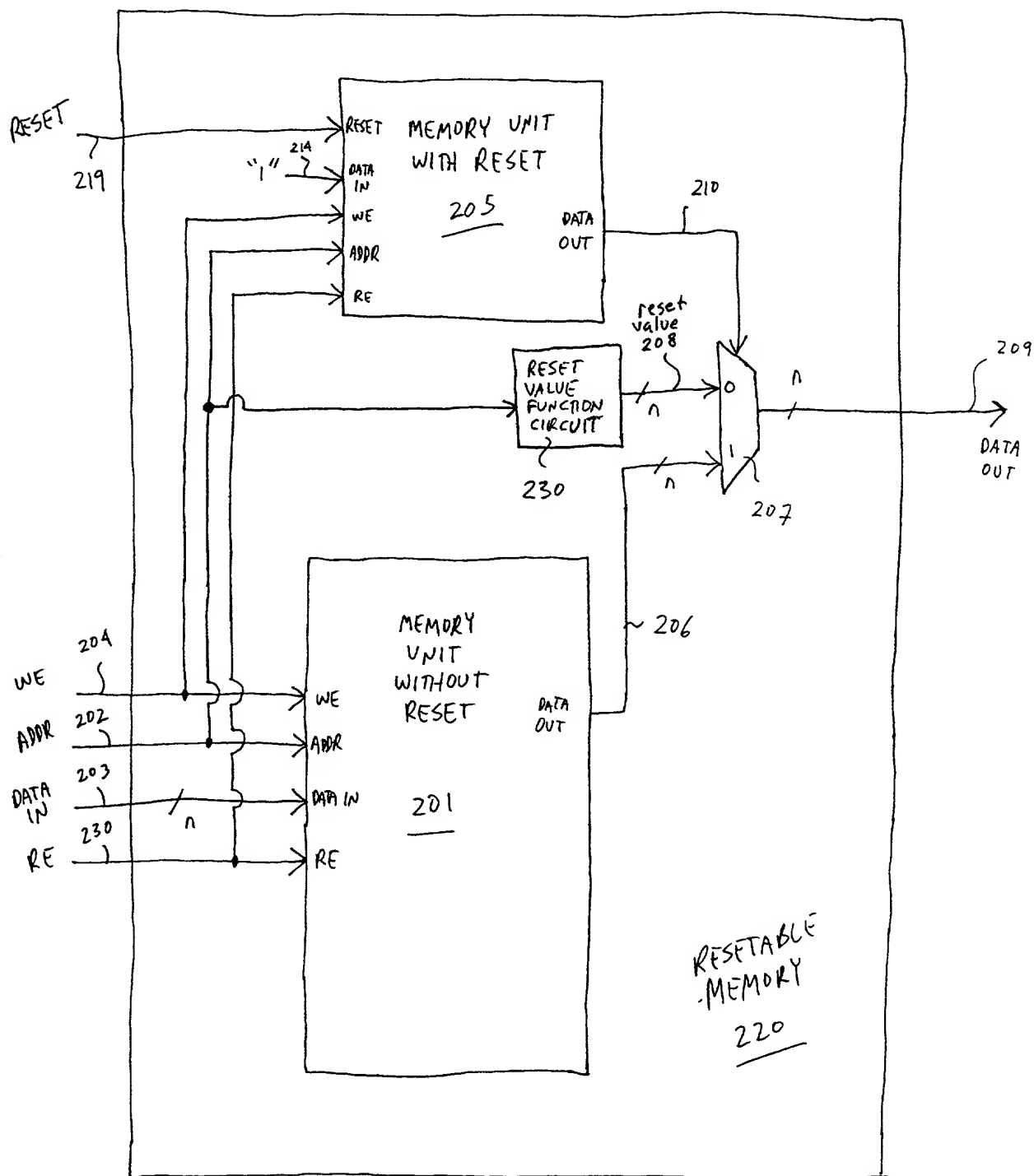


FIGURE 2B

module synReset(data_in, addr, reset, we, clk, data_out);

parameter data_width = 1024;

parameter addr_width = 10;

parameter RAMsize = 8;

parameter reset_value = 8'D0;

input [data_width-1:0] data_in;

input [addr_width-1:0] addr;

input reset, we, clk;

output [data_width-1:0] data_out;

integer i;

reg [data_width-1:0] mem [RAMsize-1:0];

wire [data_width-1:0] data_out;

//synthesis loop_limit 2000

always @(posedge clk)

begin

if(reset == 1'b1)

begin

for (i=0; i < RAMsize ; i=i+1)

begin

 mem[i] = reset_value;

end

end else if(we == 1'b1)

begin

 mem[addr] = data_in;

end

end

assign data_out = mem[addr];

endmodule

FIGURE 2C

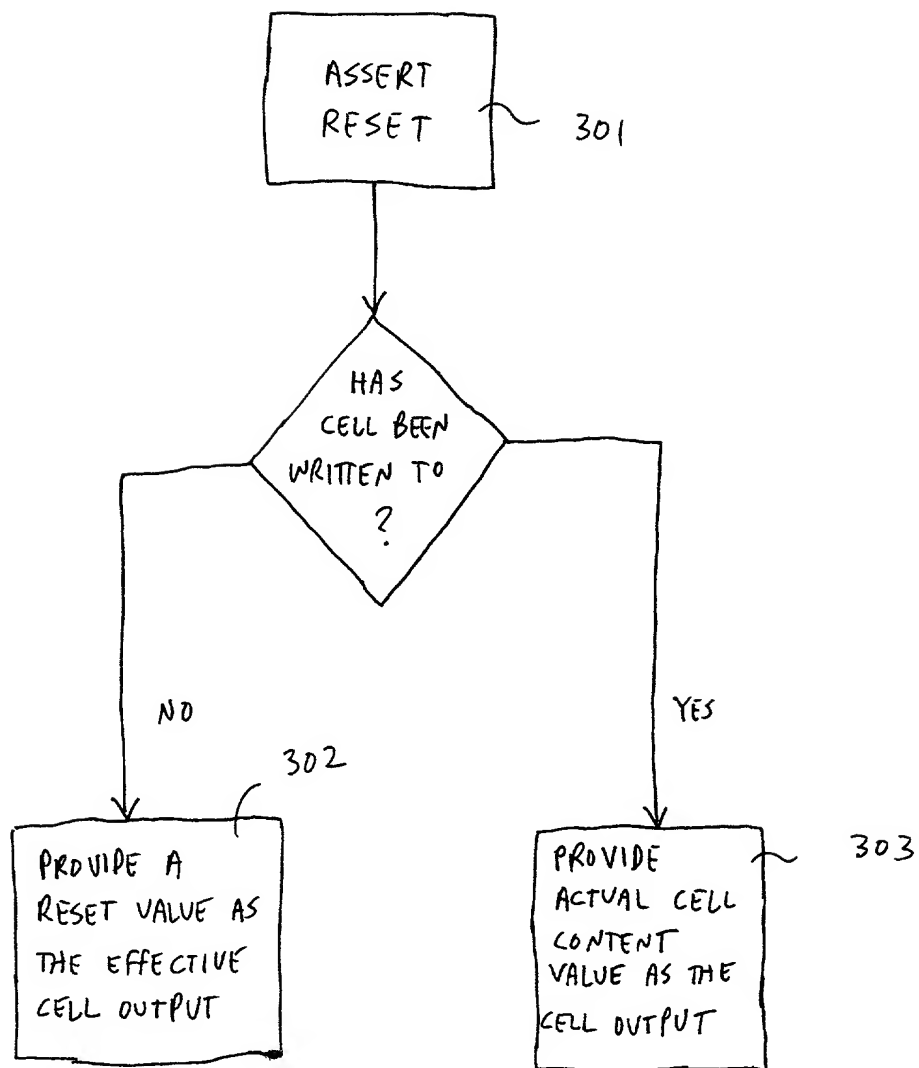


FIGURE 3

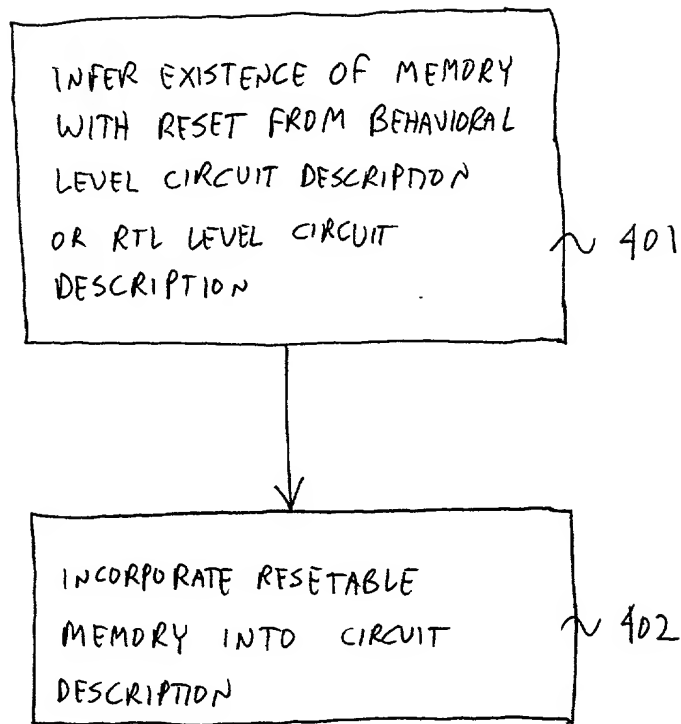


FIGURE 4

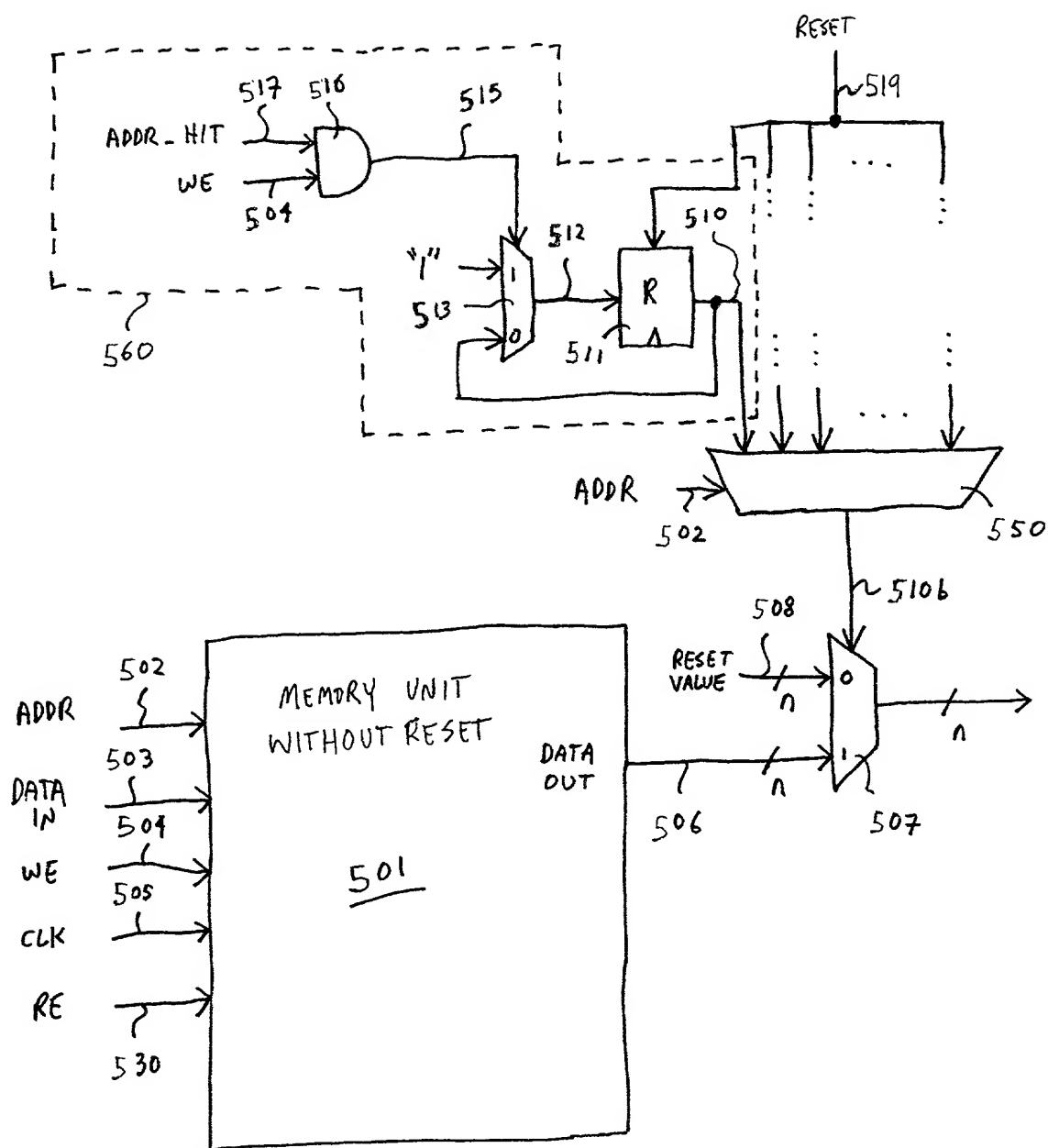


FIGURE 5

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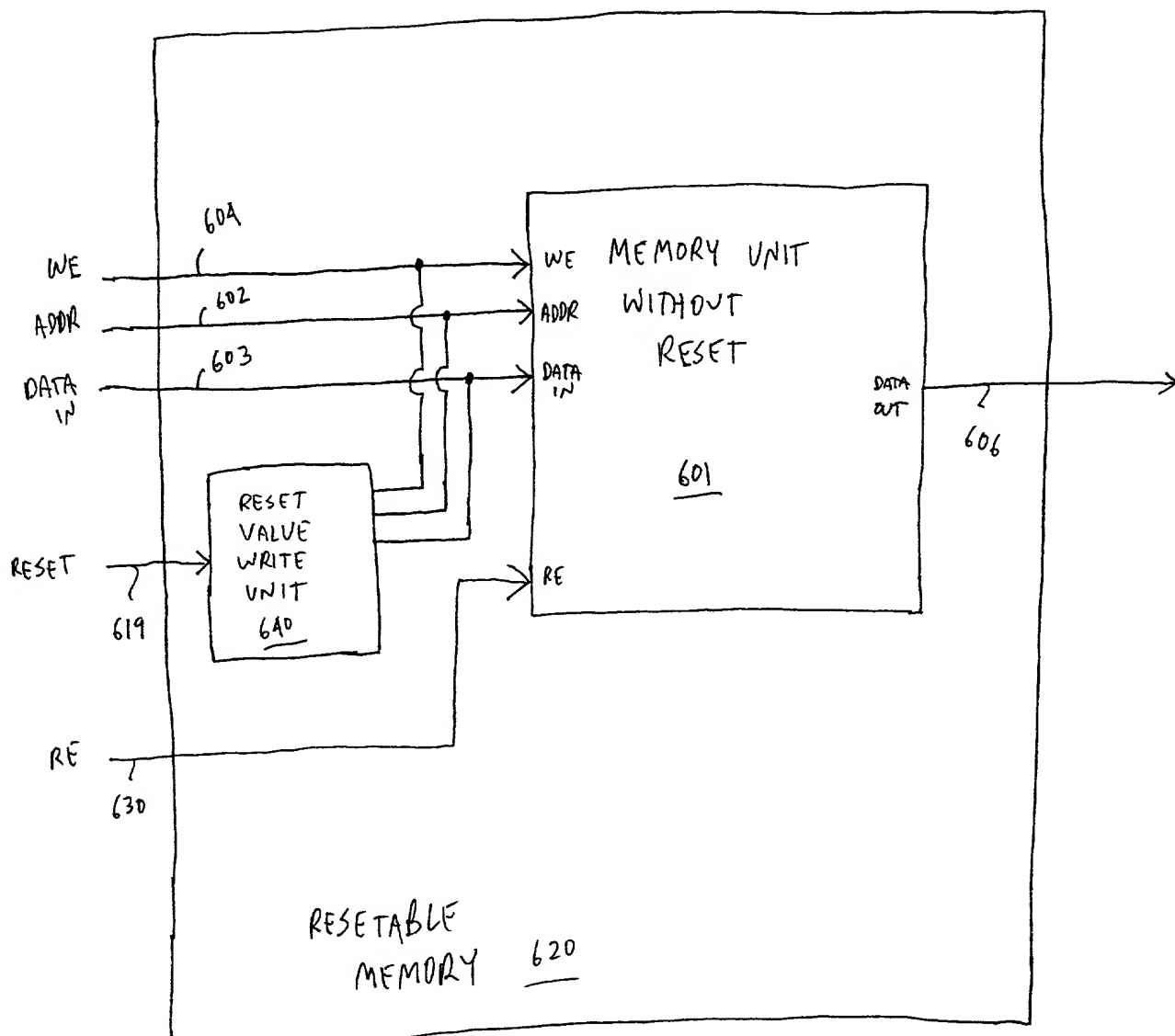


FIGURE 6

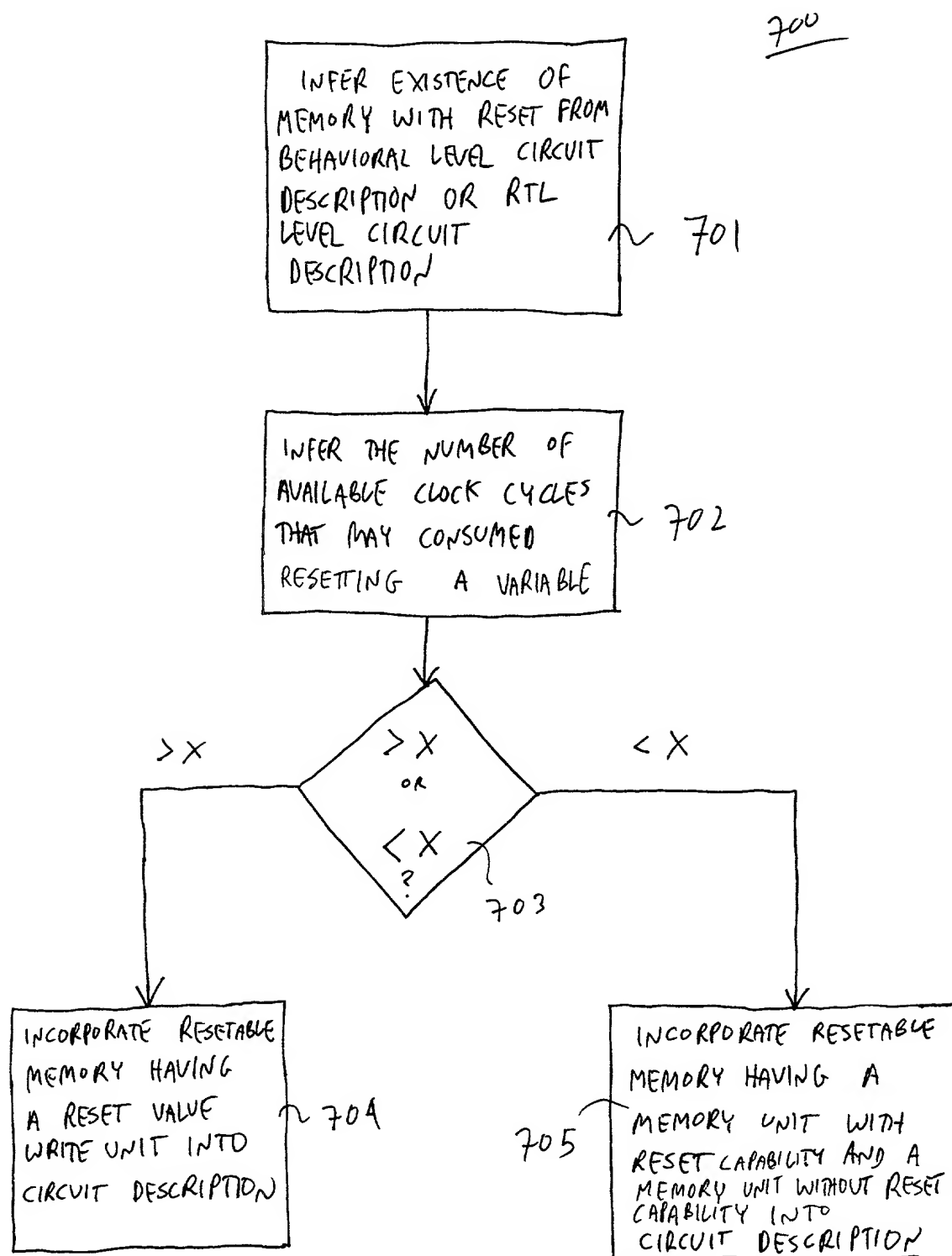


FIGURE 7

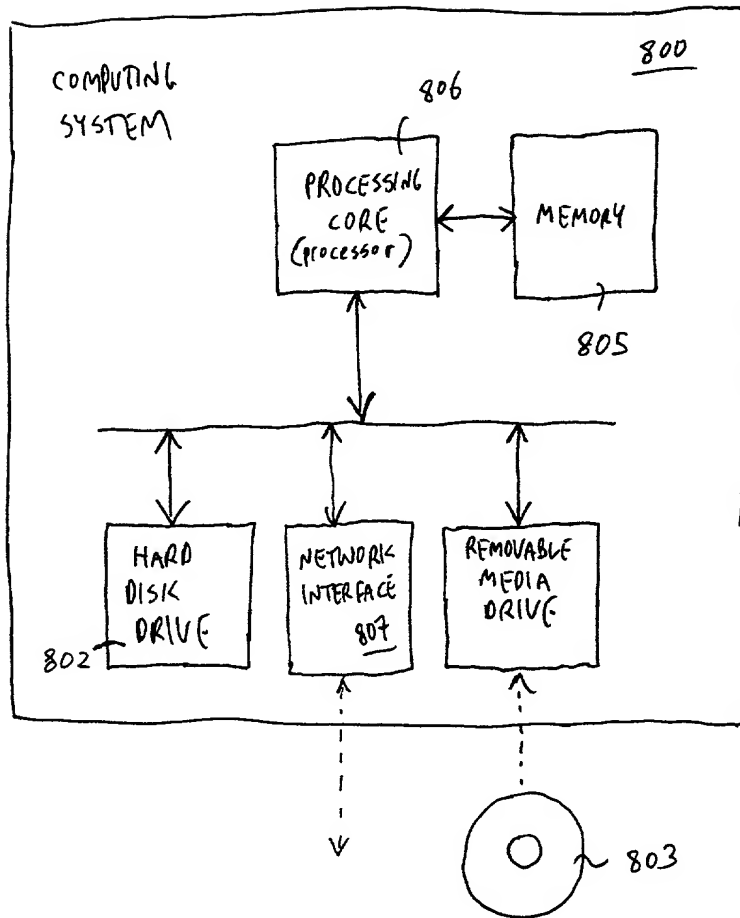


FIGURE 8